

CLAIMS:

1. A method for reducing an etch rate of a silicon-comprising material comprising incorporating carbon into the material to form a carbon-containing material.

2. The method of claim 1 wherein the incorporating carbon comprises incorporating the carbon into the material to an amount wherein the carbon-containing material comprises from about 2% to about 20% carbon (by weight).

3. The method of claim 1 wherein the incorporating carbon comprises providing implanting carbon into the material.

4. The method of claim 1 wherein the silicon-comprising material is formed by CVD in a CVD reactor, and wherein the incorporating carbon comprises providing a carbon-containing gas in the CVD reactor during formation of the silicon-comprising material.

5. The method of claim 4 wherein the carbon-containing gas comprises one or more of tetraethylorthosilicate, bis-(tertiary butyl amino)silane, methane, carbon dioxide, or carbon tetrachloride.

1 6. The method of claim 4 wherein the silicon-comprising
2 material comprises silicon nitride; and wherein the carbon-containing gas
3 comprises one or more of tetraethylorthosilicate, bis-(tertiary butyl
4 amino)silane, methane, carbon dioxide, or carbon tetrachloride.


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6 7. The method of claim 1 wherein the silicon-comprising
7 material comprises silicon nitride.

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9 8. The method of claim 1 wherein the silicon-comprising
10 material comprises silicon oxide.

11
12 9. An etching process comprising:
13 exposing a first silicon-comprising material and a second
14 silicon-comprising material to etching conditions selective for etching the
15 first silicon-comprising material relative to the second silicon-comprising
16 material, the second silicon-comprising material comprising silicon,
17 nitrogen, and carbon; and

18 the second silicon-comprising material etching at a rate that is less
19 than or equal to about 5Å per second during said exposing.
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1 10. The etching process of claim 9 wherein the second
2 silicon-comprising material etches at rate of less than or equal to about
3 2Å per second.

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5 11. The etching process of claim 9 wherein the second
6 silicon comprising material comprises from about 2% to about 20%
7 carbon (by weight). 

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9 12. The etching process of claim 9 wherein the first silicon-
10 comprising material comprises silicon and oxygen, and wherein the
11 second silicon-comprising material comprises silicon, oxygen, and carbon.

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13 13. The etching process of claim 12 wherein the second silicon-
14 comprising material comprises from about 2% to about 20% carbon (by
15 weight).

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17 14. The etching process of claim 9 wherein the first silicon-
18 comprising material comprises BPSG, and wherein the second silicon-
19 comprising material comprises silicon nitride and carbon.

15. The etching process of claim 9 wherein the first silicon-comprising material comprises BPSG, and wherein the second silicon-comprising material comprises silicon dioxide and carbon.

16. An etching process, comprising:
providing a first material over a substrate, the first material comprising from about 2% to about 20% carbon (by weight);
providing a second material over the first material; and
etching the second material at a faster rate than the first material.

17. The method of claim 16 wherein the first material comprises silicon carbide.

18. The method of claim 16 wherein the first material comprises silicon, oxygen and the carbon.

19. The method of claim 16 wherein:
the first material comprises silicon, oxygen and the carbon; and
the second material comprises silicon and oxygen.

1 20. The method of claim 16 wherein the first material consists
2 essentially of silicon, oxygen and the carbon.

3
4 21. The method of claim 16 wherein the first material comprises
5 silicon, nitrogen and the carbon.

6
7 22. The method of claim 16 wherein:
8 the first material comprises silicon, nitrogen and the carbon; and
9 the second material comprises silicon and oxygen.

10
11 23. The method of claim 16 wherein the first material consists
12 essentially of silicon, nitrogen and the carbon.

13
14 24. A method of forming an opening, comprising:
15 forming an etch stop layer over a substrate, the etch stop layer
16 comprising carbon;

17 forming an insulative layer over the etch stop layer; and
18 etching through the insulative layer utilizing conditions selective
19 for etching the insulative layer at a faster rate than the etch stop layer
20 to form an opening through the insulative layer to the etch stop layer.

1 25. The method of claim 24 wherein the insulative layer
2 comprises BPSG, wherein the etch stop layer comprises silicon nitride
3 and carbon, and wherein the BPSG has a thickness less than
4 1.3 microns before the etch.

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6 26. The method of claim 24 wherein the etch stop layer
7 comprises silicon, oxygen and the carbon.

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9 27. The method of claim 24 wherein the etch stop layer
10 comprises silicon, nitrogen and the carbon.

11
12 28. A method of forming silicon nitride comprising incorporating
13 carbon at a concentration of from about 2% to about 20% (by weight)
14 within the silicon nitride.

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16 29. The method of claim 28 wherein the incorporating carbon
17 comprises providing implanting carbon into the silicon nitride.

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19 30. The method of claim 28 wherein the silicon nitride is
20 formed by CVD in a CVD reactor, and wherein the incorporating
21 carbon comprises providing a carbon-containing gas in the CVD reactor
22 during formation of the silicon nitride.
23

1 31. The method of claim 30 wherein the carbon-containing gas
2 comprises one or more of tetraethylorthosilicate, bis-(tertiary butyl
3 amino)silane, methane, carbon dioxide, or carbon tetrachloride.
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5 32. A capacitor forming method, comprising:
6 forming a wordline over a substrate, the wordline having a
7 sidewall;

8 forming an insulative spacer along the sidewall;

9 forming an etch stop layer over the wordline and over the
10 insulative spacer; at least one of the etch stop layer and the insulative
11 spacer comprising carbon;

12 forming an insulative layer over the etch stop layer;

13 etching through the insulative layer to the etch stop layer to form
14 an opening through the insulative layer; and

15 forming a capacitor construction comprising a storage node,
16 dielectric layer and second electrode, at least a portion of the capacitor
17 construction being within the opening.
18

19 33. The method of claim 32 wherein the at least one of the
20 etch stop layer and the sidewall spacer comprises from about 2% carbon
21 to about 20% carbon (by weight).
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1 34. The method of claim 32 wherein the sidewall spacer
2 comprises silicon, oxygen and the carbon.

3
4 35. The method of claim 32 wherein the etch stop layer
5 comprises silicon, oxygen and the carbon.

6
7 36. The method of claim 32 wherein the etch stop layer
8 comprises silicon, nitrogen and the carbon.

9
10 37. The method of claim 32 wherein:
11 the etch stop layer comprises silicon, nitrogen and the carbon; and
12 the sidewall spacer consists essentially of silicon and oxygen.

13
14 38. The method of claim 32 wherein:
15 the etch stop layer consists essentially of silicon and nitrogen; and
16 the sidewall spacer comprises silicon, oxygen and carbon.

17
18 39. The method of claim 32 wherein the at least one of the
19 etch stop layer and the sidewall spacer comprises silicon, oxygen and the
20 carbon.

1 40. The method of claim 32 wherein the at least one of the
2 etch stop layer and the sidewall spacer consists essentially of silicon,
3 oxygen and the carbon.

4
5 41. The method of claim 32 wherein the at least one of the
6 etch stop layer and the sidewall spacer comprises silicon, nitrogen and
7 the carbon.

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9 42. The method of claim 32 wherein the at least one of the
10 etch stop layer and the sidewall spacer consists essentially of silicon,
11 nitrogen and the carbon.

1 43. A capacitor forming method, comprising:
2 forming a wordline over a substrate;
3 defining a node proximate the wordline;
4 forming an etch stop layer over the wordline, the etch stop layer
5 comprising carbon;
6 forming an insulative layer over the etch stop layer;
7 etching through the insulative layer to the etch stop layer to form
8 an opening through the insulative layer; and
9 forming a capacitor construction comprising a storage node,
10 dielectric layer and second electrode, at least a portion of the capacitor
11 construction being within the opening.

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13 44. The method of claim 43 further comprising etching through
14 the etch stop layer and to the node proximate the wordline prior to
15 forming the capacitor construction.

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17 45. The method of claim 43 wherein the etch stop layer
18 comprises from about 2% carbon to about 20% carbon (by weight).

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20 46. The method of claim 43 wherein the etch stop layer
21 comprises silicon, oxygen and the carbon.
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1 47. The method of claim 43 wherein the etch stop layer consists
2 essentially of silicon, oxygen and the carbon.

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4 48. The method of claim 43 wherein the etch stop layer
5 comprises silicon, nitrogen and the carbon.

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7 49. The method of claim 43 wherein the etch stop layer consists
8 essentially of silicon, nitrogen and the carbon.
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1 50. A DRAM forming method comprising:
2 forming a pair of wordlines over a substrate;
3 defining three nodes proximate the wordlines, the three nodes
4 comprising a first node, second node and third node; the second node
5 being in gated electrical connection with the first node through one of
6 the wordlines and being in gated electrical connection with the third
7 node through the other of the wordlines;
8 forming an etch stop proximate the wordlines, the etch stop
9 comprising carbon;
10 forming an insulative layer over the etch stop;
11 forming first, second and third openings extending through the
12 insulative layer, the forming the first second and third openings
13 comprising etching through the insulative layer to the etch stop;
14 forming a first capacitor construction in electrical connection with
15 the first node;
16 forming a second capacitor construction in electrical connection
17 with the third node; and
18 forming a bit line contact in electrical connection with the second
19 node.
20

21 51. The method of claim 50 wherein the etch stop is formed
22 over the wordlines.
23

1 52. The method of claim 50 wherein the etch stop is formed
2 adjacent the wordlines as sidewall spacers along sidewall edges of the
3 wordlines.

4
5 53. The method of claim 50 wherein the etch stop comprises
6 silicon, oxygen and carbon.

7
8 54. The method of claim 50 wherein the etch stop comprises
9 silicon, oxygen and nitrogen.

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11 55. The method of claim 50 further comprising, before forming
12 the first capacitor construction, etching through the etch stop to expose
13 the first node.

14
15 56. The method of claim 50 further comprising, before forming
16 the bit line contact, etching through the etch stop to expose the second
17 node.

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19 57. The method of claim 50 further comprising, before forming
20 the second capacitor construction, etching through the etch stop to
21 expose the second node.
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1 58. The method of claim 50 wherein the forming the first,
2 second and third openings occurs simultaneously in a common etch.

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4 59. The method of claim 50 wherein the forming the at least
5 one of the first, second and third openings occurs sequentially in a
6 separate etch from forming the others of the first, second and third
7 openings.

8
9 60. A semiconductive material assembly, comprising:
10 a semiconductive substrate; and
11 a layer over the semiconductive substrate, the layer comprising
12 silicon, nitrogen and carbon.

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14 61. The assembly of claim 60 wherein the layer comprises from
15 about 2% carbon to about 20% carbon (by weight).

16
17 62. The assembly of claim 60 wherein the layer consists
18 essentially of silicon, nitrogen and carbon.

19
20 63. The assembly of claim 60 wherein the layer consists
21 essentially of silicon, nitrogen and carbon and comprises from about 2%
22 carbon to about 20% carbon (by weight).
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1 64. A wordline construction, comprising:
2 a conductive gate having sidewalls; and
3 sidewall spacers extending along the sidewalls of the conductive
4 gate, the sidewall spacers having thicknesses of less than or equal to
5 about 500Å.
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7 65. The wordline of claim 64 wherein the sidewall spacers
8 comprise from about 2% to about 20% carbon (by weight).
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10 66. The wordline of claim 65 wherein the sidewall spacers
11 further comprise silicon and oxygen.
12

13 67. The wordline of claim 65 wherein the sidewall spacers
14 further comprise silicon and nitrogen.
15

16 68. A capacitor construction, comprising:
17 a storage node extending within an insulative layer, at least a
18 portion of the storage node extending along and against a material that
19 comprises carbon;
20 a second electrode proximate the storage node; and
21 a dielectric layer between the second electrode and the storage
22 node.
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1 69. The capacitor construction of claim 68 wherein the material
2 comprises from about 2% carbon to about 20% carbon (by weight).
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4 70. The capacitor construction of claim 68 wherein the material
5 comprises silicon, oxygen and carbon.
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7 71. The capacitor construction of claim 68 wherein the material
8 comprises silicon carbide.
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10 72. The capacitor construction of claim 68 wherein the material
11 comprises silicon, oxygen and the carbon.
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13 73. The capacitor construction of claim 68 wherein the material
14 consists essentially of silicon, oxygen and the carbon.
15

16 74. The capacitor construction of claim 68 wherein the material
17 comprises silicon, nitrogen and the carbon.
18

19 75. The capacitor construction of claim 68 wherein the material
20 consists essentially of silicon, nitrogen and the carbon.
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1 76. A DRAM construction, comprising:
2 a pair of wordlines over a substrate, the wordlines comprising
3 sidewall edges;
4 three nodes proximate the wordlines, the three nodes comprising
5 a first node, second node and third node, the second node being in
6 gated electrical connection with the first node through one of the
7 wordlines and being in gated electrical connection with the third node
8 through the other of the wordlines;
9 a carbon-containing material proximate the wordlines;
10 an insulative layer over the etch stop;
11 a first capacitor construction in electrical connection with the first
12 node, the first capacitor construction comprising a first storage node;
13 a second capacitor construction in electrical connection with the
14 third node, the second capacitor construction comprising a second
15 storage node; and
16 a bit line contact in electrical connection with the second node,
17 at least one of the first storage node, second storage node and bit line
18 contact being in physical contact with the carbon-containing material.

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20 77. The DRAM construction of claim 76 wherein the carbon-
21 containing material is over the wordlines.
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1 78. The DRAM construction of claim 76 wherein the carbon-
2 containing material is over the wordlines and comprises silicon, nitrogen
3 and carbon.

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5 79. The DRAM construction of claim 76 wherein the carbon-
6 containing material is adjacent the wordlines as sidewall spacers along
7 sidewall edges of the wordlines.

8
9 80. The DRAM construction of claim 76 wherein the carbon-
10 containing material is adjacent the wordlines as sidewall spacers along
11 sidewall edges of the wordlines and comprises silicon, oxygen and
12 carbon.

13
14 81. The DRAM construction of claim 76 wherein the carbon-
15 containing material comprises silicon carbide.

16
17 82. The DRAM construction of claim 76 wherein the carbon-
18 containing material comprises from about 2% carbon to about 20%
19 carbon (by weight).

20
21 83. The DRAM construction of claim 76 wherein the carbon-
22 containing material comprises silicon, oxygen and carbon.
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1 *sub 17* 84. The DRAM construction of claim 76 wherein the carbon-
2 containing material consists essentially of silicon, oxygen and carbon.

3
4 85. The DRAM construction of claim 76 wherein the carbon-
5 containing material comprises silicon, oxygen and nitrogen.

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7 86. The DRAM construction of claim 76 wherein the carbon-
8 containing material consists essentially of silicon, oxygen and nitrogen.

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14 Add E3 >

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16 ADD F3 >